UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/398,189	09/17/1999	JUN KANAMORI	IIZ.008D	9755

7590 08/12/2002

JONES VOLENTINE LLP
12200 SUNRISE VALLEY DRIVE STE 150
RESTON, VA 20191

EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,189	KANAMORI, JUN	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *2-6, 24 -30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). 22 .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' amendment filed on July 23, 2002 was entered on August 01, 2002.

Therefore claims 2-6 and 24-29 as recited in the amendment are currently pending in the application. Claim 30 was newly added by the amendment. Claim 23 has been cancelled by the amendment.

Finality of the Office Action

The previous Office Action mailed on April 29, 2002 was a Final Action(herein after Final rejection) . The Finality of the Office Action was based on the fact that that the same references as previously applied were also used in the Final rejection.

Applicants' argue that the finality was premature because the 112 first paragraph rejection of claim 24 was premature because it (claim 24) previously (i.e. in the preliminary amendment of July 21, 2201) contained the language ("a first annealing" and " second annealing").

The Final rejection actually rejected claims 23, 24 and 6 under section 112 first paragraph. A review of Applicants' amendments dated July 12, 2001 and February 04, 2002 shows beyond any doubt that at least with respect to claim 6 the language " second annealing" was added for the first time by the amendment of February 04, 2002.

Therefore Applicants' amendment filed July 23, 2002 is non-responsive because it fails to address the 112 issues with regard to claims 23 and 6. As claim 23 is cancelled by the amendment the issue with respect to claim 23 is moot. However claim 6 is still pending and failure to address the 112 first paragraph rejection makes the amendment filed July 23, 2002 non responsive.

However, with a view to move the case forward, and to reduce the issues in the event of an appeal, the incomplete response is entered and a Second Final rejection is being mailed.

Claim Rejections - 35 USC § 112

As applicants' have amended claims 6 and 24 to replace "annealing" with " rapid thermal annealing" and the newly added claim 30 uses the above RTA instead of the term " annealing" , upon entering of this amendment applicants' would have over come the 112 first paragraph rejection.

There fore as all pending claims only recite " first rapid thermal annealing" and "second rapid thermal annealing" the 112 first paragraph rejection is withdrawn.

Information Disclosure Statement

Applicants' contend that page 1 of the present application provides the concise explanation required by 37 CFR 1.98 (a) (3).

Applicants' page 1 states, " As shown in "Semiconductor World", May 1998, page 66, salicide process has been used to decrease that resistance. Especially for SOI (Silicon-On-Insulator) type of devices, the salicide process is important".

Applicants' have enclosed pages 66-70 of the said article. It is clear that from the previous rejection (O/A mailed 10/02/01) stated, " The information disclosure statement filed September 17, 1999 fails to comply with 37 CFR 1.98(a) (3) because it does not include a concise explanation of the relevance, as it is presently understood by

the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not I English Language. It has been placed in the application file, but referred to therein has not been considered"..

It is noted that 37 CF R 1.98 (a) (3) (ii) states, "A copy of the translation if a written English-language translation of a non-English-language document, or portion thereof, is within the possession, custody, or control of, or is readily available to any individual designated in § 1.56(c)."

The Examiner requested a more detailed English translation , to determine the complete relevancy of the reference, as the one line explanation in the application does not convey all the important points of a four page document.

However, again with a view to move the case forward, the Examiner has requested an in house translation from Japanese in to English of the document to review the entire contents of the document and upon receipt of the translation the Examiner will certainly consider the reference and a copy of the initialed 1449 will be mailed/faxed to the applicants' representative.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-6 and 24-29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPR (Applicants' Admitted Prior Art), Doan (U.S. Patent No. 5,946,595, herein after Doan) and Besser et al. (U.S. Patent No. 6,165,903, herein after Besser) and Xiang (U.S. Patent No. 6,015,752 , herein after Xiang) .

With respect to newly added claim 30, AAPR teaches the method of fabricating a semiconductor device including the steps of :

Providing a silicon substrate (AAPR fig. 1 # 12), providing a buried oxide layer on the silicon substrate (AAPR fig.1 # 14), providing a filed oxide layer and a silicon on insulator layer on the buried oxide layer (AAPR # 16 and 18)providing a gate oxide layer on the silicon on insulator layer (AAPR # 20), providing a poly-silicon gate layer on the gate oxide layer (AAPR # 22), providing a gate sidewall layer on the silicon on insulator layer to surround the poly-silicon gate layer and the gate oxide layer (AAPR # 24), providing a material to be silicided on a surface of the semiconductor device including the poly silicon gate layer, the gate sidewall layer, the silicon on insulator layer and the field oxide layer (AAPR fig. 1B and C ultimately forming layer 32), performing a first rapid thermal annealing process to from first-reacted silicide regions in the poly-silicon gate layer and in source/drain active areas of the silicon on insulator layer (AAPR Applicants' specification –prior art section page 2 lines 9-14), removing non-reacted material from the first –reacted silicide regions (AAPR specification –prior art section page 2 lines 13-15).

"Providing a supplemental silicon layer over the surface of the semiconductor device after the non-reacted material is removed. "

The AAPR does not specifically describe providing a supplemental silicon layer over the surface of the semiconductor device after the non-reacted material is removed.

However, Besser, a patent from the same filed of invention, describes in fig. 8 layer # 46 and col. 5 lines 25-40 to convert the first reacted silicide region into a second reacted silicide region and to prevent junction leakage problem.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Beesser's second supplemental silicon layer in AAPR"s method steps to prevent junction leakage problem. (Besser col. 5 lines 65-col. 6 line 5).

"Doping the supplemental silicon layer".

AAPR and Besser do not specifically describe doping the supplemental silicon layer.

However, Doan, a patent from the same filed of endeavor, describes in fig. 8 and col. 6 lines 7-17 the doping of the supplemental silicon layer so that it can etched at a faster rate in comparison with the layers below it.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Doan's doping of the supplemental silicon layer step in AAPR , Besser's method to provide a doped layer that etches differently from the layers underlying it. (Doan col. 6 lines 31-37).

The supplemental silicon region preventing the poly-silicon gate layer and the silicon on insulator layer from being completely silicided (Doan col. 6 lines 36-39 and further as Doan and the instant application use the same materials in similar method steps for the same purpose what is true for applicants is also true for Doan).

"The semiconductor device including a p-channel MOS transistor having a p-type source and rain regions, and including an n-channel MOS transistor having n-type source and drains. "

AAPR, Besser and Doan do not specifically describe a CMOS device .

However, Xiang, col. 3 line 47, col.5 line 59-60 was cited to show that by definition (and as is well known to one of ordinary skill in the art) CMOS includes both n-channel transistor having n-type source and drain regions and p-channel transistors having p-type source and drain regions.

"Said doping comprising doping a p-type impurity into the supplemental silicon that is provided over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is provided over the n-channel Mos transistor. "

Further a p-type source/drain with a thin polysilicon strap (as shown in Doan i.e the supplemental silicon layer) would obviously have to be doped p-type to form an excellent ohmic contact and avoidance of a P-N diode formation and similarly for N-type source/drain region the connecting strap (the thin poly silicon strap, i.e. supplemental silicon layer) would be doped N-type for the same reasons.

Therefore all the presently recited steps in the method of fabricating the semiconductor device of claim is obvious in vie w of the prior art of record for the reasons stated above.

Dependent claims 2-6 claims were alleged to be allowable because they depend from allegedly allowable claim 30.

However as shown above claim 30 is not allowable therefore claims 2-6 are also not allowable and are rejected for reasons set out previously and those set out above.

Applicants' alleged that claim 24 was not obvious for some what similar reasons as set forth above, namely the prior art does not disclose doping a p-type impurity in to a supplemental layer formed over a p-channel MOS transistor, and doping an n-type impurity into a supplemental layer formed over an n-channel MOS transistor.

The argument is not persuasive for reasons set out in detail above and briefly stated as the prior art references applied shows a CMOS which has p-channel and n-channel MOS transistors. Further the p-channel and n-channel transistors should form good ohmic contacts to the doped polysilicon straps and avoid formation of N-P/P-N diodes.

No specific arguments are made with respect to claims 25-29, however they are rejected for reasons previously set out and those set out above.

Response to Arguments

Applicant's arguments filed 7/29/01 have been fully considered but they are not persuasive for the following reasons.

Applicants' are alleging non obviousness based on piece meal analysis of the references, it is well settled law that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on the combinations of references.

Applicants' first argue that, "Applicant's prior art figs. 1a-1c do not include a supplemental silicon layer ".

It is noted that the rejection is over the combined teachings of AAPR, Doan and Besser.

As stated in the Office Action mailed 10/02/01 Besser in fig. 8 col. 5line 49-col. 6 line 56 describes a second supplemental silicon layer 46. Additionally, Doan layer 24 is a second supplemental silicon layer.

Applicants' next argue that, " However, polysilicon layer 24 of the Doan et al. reference is not describes or suggested as being doped with an impurity".

However, Doan in fig. 8 reproduced below shows :

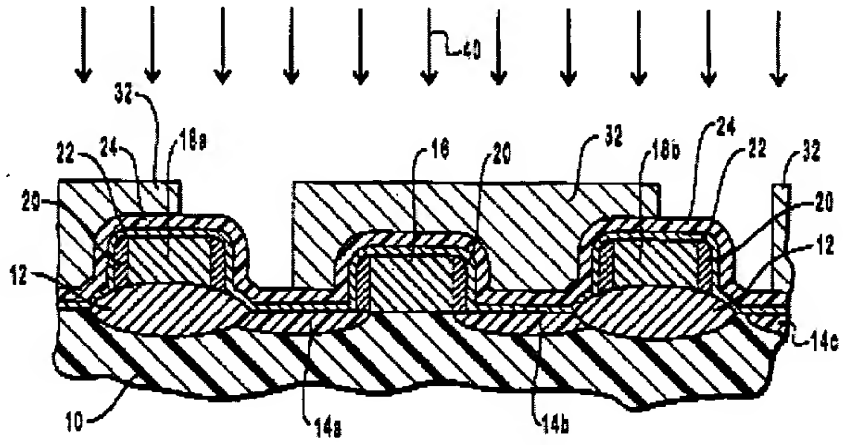

FIG. 8

and in col. 6 lines 17 to 30 describes :

> The next step in the method of the present invention is to implant ions, represented by arrows **40** in FIG. **8**, into the portions of polysilicon layer **24** which are left exposed and uncovered by implant mask **32**. The ions are of a type that preferably comprises a common silicon and polysilicon dopant such as arsenic, phosphorus, argon, or boron. The ions are implanted with an implantation dose in a range from about 1×10^{13} ions per square centimeter to about 1×10^{17} ions per square centimeter. Preferably, the implantation dose is selected to result in approximately 1×10^{15} ions per square centimeter. The implantation energy is selected according to the thickness of polysilicon layer **24**, as is commonly known in the art.

Therefore Doan shows and describes polysilicon layer 24 (i.e. the supplemental silicon layer) as being doped with either p-type (boron) or n-type impurity (Phosphorus, argon , etc.) .

Applicant next argue that Doan does not describe, " doping polysilicon layer 24 with a p-type impurity over a p-channel MOS transistor and with an n-type impurity over an n-channel MOS transistor.

It is noted again that the rejection was based upon the combination of references and not a single reference.

Further, it is well known that in CMOS there are p-channel MOS transistor and a n-type MOS transistor.

Further a p-type source/drain with a thin polysilicon strap (as shown in Doan i.e the supplemental silicon layer) would obviously have to be doped p-type to form an excellent ohmic contact and avoidance of a P-N diode formation and similarly for N-type source/drain region the connecting strap (the thin poly silicon strap, i.e. supplemental silicon layer) would be doped N-type for the same reasons.

Therefore the combined teachings of the applied references teaches all the limitations of the recited claims

Applicants' next argue that the Besser et al. reference, " is not described as being doped with an impurity. More particularly silicon layer 46 is not described as being doped with a p-type impurity over a p-channel MOS transistor and an n-type impurity over an n-channel MOS transistor.

It is noted again that the rejection was based upon the combination of references and not a single reference.

For reasons set out above the combination of AAPR, Doan and Besser describes all the recited steps of the claimed method.

Applicants' next argue individually against the Xiang reference for rejection based on the combination of AAPR, Doan, Beeser and Xiang.

Applicants' allege, " Since the Xiang et al. reference doe s not include a supplemental silicon layer, the Xiang et al. reference clearly would provide no motivation to modify the previously relied upon prior art to impurity dope a supplemental silicon layer."

Applicants' argument is a misstatement of the rejection.

The rejection (in relevant parts stating Xiang was used) was in response to Applicants' arguments on page 8 of their response of Feb. 04, 2002 wherein it was alleged that the references applied in the 10/02/01 rejection did not show a structure including both a p-channel MOS transistor and a n-channel MOS transistor.

The referenced portion of Xieng (col. 3 line 47, col.5 line 59-60) was cited to show that by definition (and as is well known to one of ordinary skill in the art) CMOS includes both n-channel and p-channel transistors.

Further, Xaing in fig.. 3 and 4 shows at least two silicon layers 13 and 30 (as shown below) i.e. layer 30 is a supplemental silicon layer.

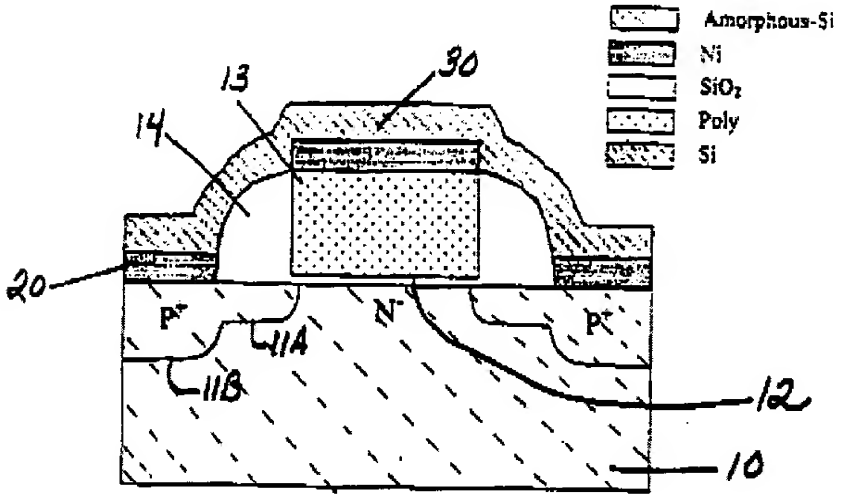

Fig.3

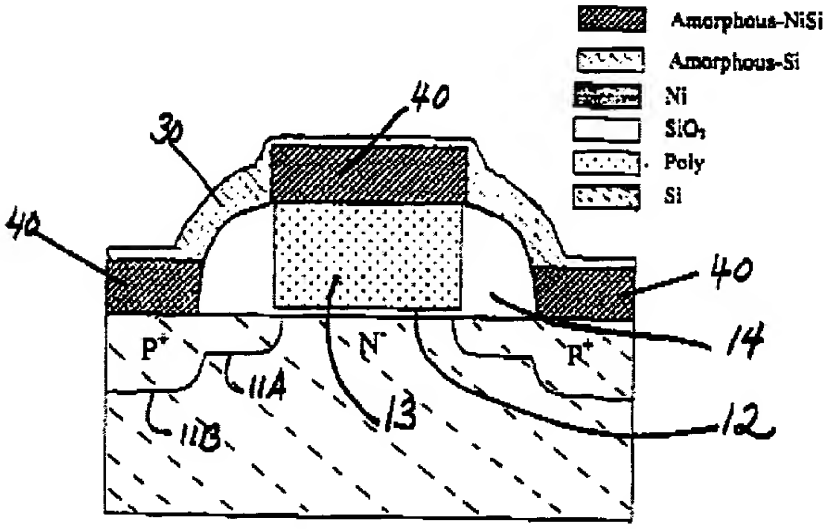

Fig.4

Next applicants' argue that Xaing does not disclose both a p-channel MOS transistor and an N-channel MOS transistor. See above Xaing (col. 3 line 47, col.5 line 59-60) was cited to show that by definition (and as is well known to one of ordinary skill in the art) CMOS includes both n-channel and p-channel transistors.

The combination of AAPR, Doan, Besser and Xaing as shown above discloses/suggests doping of a supplemental silicon layer with a p-type impurity over a p-channel Mos Transistor and a n-type impurity over a n-channel Mos transistor.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

As the same references as previously applied are also used here this forms a separate basis for making action Final.

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

August 1, 2002.

JEROME JACKSON
PRIMARY EXAMINER